# METHOD OF MAKING HIGH-VOLTAGE BIPOLAR/CMOS/DMOS (BCD) DEVICES

## Background of the Invention

1. Field of the Invention

[0001] This invention relates to the field of integrated circuit fabrication, and in particularly to a method of making high-voltage bipolar/CMOS/DMOS (BCD) devices.

2. Description of Related Art

[0002] Bipolar/CMOS/DMOS (BCD) devices are employed in high voltage applications. They typically use a Silicon On Insulator (SOI) substrate or a complex epitaxial substrate combining at least two layers of two different types of dopant, N-Type and P-Type and a very complex sequence of masks to produce the required transistors and other active components. They only provide a partial combination of standard and high-voltage transistors for the designers, require process modifications, which can be major, to fulfill various voltage operation ranges.

[0003] The following three references describe Bipolar/CMOS/DMOS (BCD) processes which require the use of a substrate combining two or more layers of different dopant types which may or may not be buried under the silicon surface: C. Contiero, P. Galbiati, M. Palmieri, L. Vecchi, "LDMOS Implemetation by Large Tilt Implant in 0.6 µm BCD5 Process, Flash Memory Compatible", International Symposium on Power Semiconductor Devices and ICs (ISPSD), 1996, pp. 75-78; US Patent No. 6,111,297 "MOS-technology power device integrated structure..."; and US Patent No. 4,795,716 "Method of making a power IC structure with enhancement..."

[0004] This BCD approach requies extra masks and processing steps for lateral isolation as well as an expensive epitaxial deposition reactor used to generate buried epitaxial layers. A major disadvantage of this approach resides in the fact that the resulting DMOS transistors are mostly vertical.

[0005] The following five references describe other Bipolar/CMOS/DMOS (BCD) processes which require the use of a Silicon-On-Insulator (SOI) substrate to integrate the high-voltage components on a oxide dielectric layer buried under the silicon surface: J.A. van der Pol, "A-BCD : An Economic 100V RESURF Silicon-On-Insulator BCD Technology for Consumer and Automotive Applications", International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2000, pp. 327-330; USA Patent No. 6,130,458 "Power IC having SOI structure"; USA Patent No. 5,939,755 "Power IC having high-side and low-side switches in an SOI..." ; US Patent No. 5,854,113 "Method for fabricating power transistor using..."; US Patent No. 5,681,761 "Microwave power SOI-MOSFET with high conductivity..."; and US Patent No. 5,578,506 "Method of fabricating improved lateral Silicon-On-Insulator..."

[0006] These BCD processes on SOI wafers using very expensive SOI substrates also add costs and additional processing steps for lateral isolation. More importantly, the high-voltage components built on SOI substrates cannot be integrated on the bulk or epitaxial wafer of our invention because some components would not be self-isolated from other components and would share common drain electrodes.

[0007] These and other Prior Art BCD processes that can be found in the literature cannot integrate high-voltage single extended NMOSFET or high-voltage double extended NMOSFET distinct from the DMOS transistor simply because these processes do not provide an isolated N-Well in a P-Type region, thus forming the required isolating junction. The resulting number of high-voltage N-Channel components is therefore reduced compared to our proposed invention.

**Summary of the Invention**

[0008] According to the present invention there is provided a process for making an integrated circuit, comprising:

a) providing a substrate or epitaxial layer of p-type material; and

b) applying a sequence of mask steps as follows:

(1) applying a first mask and forming at least one N-well in said p-type material therethrough;

(2) applying a second mask and forming an active region therethrough;

(3) applying a third mask and forming a p-type field region therethrough;

(4) applying a fourth mask and forming a gate oxide therethrough;

(5) applying a fifth mask and carrying out a p-type implantation therethrough;

(6) applying a sixth mask and forming polysilicon gate regions therethrough;

(7) applying a seventh mask and forming a p-base region therethrough;

(8) applying an eighth mask and forming a N-extended region therethrough;

(9) applying a ninth mask and forming a p-top region therethrough;

(10) applying a tenth mask and carrying out an N+ implant therethrough;

(11) applying an eleventh mask and carrying out a P+ implant therethrough;

(12) applying a twelfth mask and forming contacts therethrough;

(13) applying a thirteenth mask and depositing a metal layer therethrough;

(14) applying a fourteenth mask and forming vias therethrough;

(15) applying a fifteenth mask and depositing a metal layer therethrough; and

(16) applying a sixteenth mask and forming a passivation layer therethrough; and

wherein up to any three of mask steps 4, 7, 8, and 9 may be omitted depending on the type of integrated circuit.

**[0009]** The invention provides a lower fabrication cost and more simple Bipolar/CMOS/ DMOS (BCD) process which uses a simpler and lower cost single P-Type dopant substrate; P-Type bulk substrate or; P-Epitaxial on P+ Bulk substrate (for improved latch-up immunity); a simpler and lower cost 16- mask

sequence to produce the required layers required to produce the various transistors and other active components; allows the designer to fulfill all voltage requirements between 3.3 and 600V by simply modifying the layout of the active component of interest without having to modify the process; and provides a complete combination of forty-one (41) standard and high-voltage active components ranging from 3.3 to 600 volts on this simpler and lower cost bulk or epitaxial P-type substrate of a single P-Type dopant.

**[0010]** These include six standard MOS transistors of both conductivity types, using two different gate oxide thicknesses, namely a standard N-MOSFET with standard gate oxide, a standard N-MOSFET with high-voltage gate oxide, a standard P-MOSFET with standard gate oxide, one standard P-MOSFET with high-voltage gate oxide; a standard Junction isolated N-MOSFET with standard gate oxide, a standard Junction isolated N-MOSFET with high-voltage gate oxide; twelve mid-voltage MOS transistors of both conductivity types, using two different gate oxide thicknesses, namely a mid-voltage single extended N-MOSFET with standard gate oxide, a mid-voltage single extended N-MOSFET with high-voltage gate oxide, a mid-voltage single extended P-MOSFET with standard gate oxide, a mid-voltage single extended P-MOSFET with high-voltage gate oxide, a mid-voltage double extended N-MOSFET with standard gate oxide, a mid-voltage double extended N-MOSFET with high-voltage gate oxide, a mid-voltage double extended P-MOSFET with standard gate oxide, a mid-voltage double extended P-MOSFET with high-voltage gate oxide, a mid-voltage single extended N-LDMOSFET with standard gate oxide, a mid-voltage single extended N-LDMOSFET with high-voltage gate oxide, a mid-voltage floating source N-LDMOSFET with standard gate oxide, a mid-voltage floating source N-LDMOSFET with high-voltage gate oxide; ten high-voltage MOS transistors of both conductivity types, using two different gate oxide thicknesses, namely a high-voltage single extended N-MOSFET with standard gate oxide, a high-voltage single extended N-MOSFET with high-voltage gate oxide, a high-voltage single extended P-MOSFET with standard gate oxide, a high-voltage single

extended P-MOSFET with high-voltage gate oxide, a high-voltage double extended N-MOSFET with standard gate oxide, a high-voltage double extended N-MOSFET with high-voltage gate oxide, a high-voltage double extended P-MOSFET with standard gate oxide, a high-voltage double extended P-MOSFET with high-voltage gate oxide, a high-voltage double extended N-LDMOSFET with standard gate oxide, a high-voltage double extended N-LDMOSFET with high-voltage gate oxide; six very-high-voltage MOS transistors of both conductivity types, using two different gate oxide thicknesses, namely a very-high-voltage single extended N-LDMOSFET with standard gate oxide, a very-high-voltage single extended N-LDMOSFET with high-voltage gate oxide, avery-high-voltage single extended P-MOSFET with standard gate oxide, a very-high-voltage single extended P-MOSFET with high-voltage gate oxide, a very-high-voltage double extended P-MOSFET with standard gate oxide, a very-high-voltage double extended P-MOSFET with high-voltage gate oxide; one lateral NPN bipolar transistor; two high-voltage vertical bipolar transistors of complementary types, namely a high-voltage vertical NPN bipolar transistor, a high-voltage vertical PNP bipolar transistor, a very-high-gain vertical NPN bipolar transistor, a high-voltage N-JFET; a very-high-voltage Lateral Insulated Gate Bipolar transistor LIGBT, using two different gate oxide thicknesses, namely a very-high-voltage Lateral Insulated Gate Bipolar transistor LIGBT with standard gate oxide, and a very-high-voltage Lateral Insulated Gate Bipolar transistor LIGBT with high-voltage gate oxide.

**[0011]** Each additional mask step adds expense to a manufacturing procedure. It is indeed remarkable and highly advantageous that all these devices can be fabricated using a basic 16-mask sequence.

**Brief Description of the Drawings**

**[0012]** The invention will now be described in more detail, by way of example only, with reference to the accompanying drawings, in which:-

Figure 1 lists a basic twelve-mask CMOS process with standard gate oxide;

Figure 2 shows the number of active components associated with the various combinations of masks of standard gate oxide processes;

Figure 3 lists an N-Extended thirteen-mask CMOS process with standard gate oxide;

Figure 4 lists a P-Top thirteen-mask Bipolar/CMOS process with standard gate oxide;

Figure 5 lists a N-Extended and P-Top fourteen-mask Bipolar/CMOS process with standard gate oxide;

Figure 6 lists a P-Base thirteen-mask Bipolar/CMOS/DMOS process with standard gate oxide;

Figure 7 lists a P-Base and N-Extended fourteen-mask Bipolar/CMOS/DMOS process with standard gate oxide;

Figure 8 lists a P-Base and P-Top fourteen-mask Bipolar/CMOS/DMOS process with standard gate oxide;

Figure 9 lists a P-Base, N-Extended and P-Top fifteen-mask Bipolar/CMOS/DMOS process steps with standard gate oxide;

Figure 10 lists the number of active components associated with the various combinations of masks of dual gate oxide processes;

Figure 11 lists a dual gate oxide basic thirteen-mask CMOS process;

Figure 12 lists a dual gate oxide P-Top fourteen-mask Bipolar/CMOS process;

Figure 13 lists the dual gate oxide N-Extended fourteen-mask CMOS process;

Figure 14 lists a dual gate oxide N-Extended and P-Top fifteen-mask Bipolar/CMOS process;

Figure 15 lists a dual gate oxide P-Base fourteen-mask Bipolar/CMOS/DMOS process;

Figure 16 lists a dual gate oxide P-Base and N-Extended fifteen-mask Bipolar/CMOS/DMOS process;

Figure 17 lists the dual gate oxide P-Base and P-Top fifteen-mask Bipolar/CMOS/DMOS process steps;

Figure 18 lists a dual gate oxide P-Base, N-Extended and P-Top sixteen-mask Bipolar/CMOS/DMOS process;

Figure 19a illustrates a standard N-MOSFET with standard gate oxide;

Figure 19b illustrates a standard N-MOSFET LIGBT with high-voltage gate oxide;

Figure 20a illustrates a standard P-MOSFET with standard gate oxide;

Figure 20b illustrates a standard P-MOSFET with high-voltage gate oxide;

Figure 21a illustrates a standard Junction isolated N-MOSFET with standard gate oxide;

Figure 21b illustrates a standard Junction isolated N-MOSFET with high-voltage gate oxide;

Figure 22a illustrates a mid-voltage single extended N-MOSFET with standard gate oxide;

Figure 22b illustrates a mid-voltage single extended N-MOSFET with high-voltage gate oxide;

Figure 23a illustrates a mid-voltage single extended P-MOSFET with standard gate oxide;

Figure 23b illustrates a mid-voltage single extended P-MOSFET with high-voltage gate oxide;

Figure 24a illustrates a mid-voltage double extended N-MOSFET with standard gate oxide;

Figure 24b illustrates a mid-voltage double extended N-MOSFET with high-voltage gate oxide;

Figure 25a illustrates a mid-voltage double extended P-MOSFET with standard gate oxide;

Figure 25b illustrates a mid-voltage double extended P-MOSFET with high-voltage gate oxide;

Figure 26a illustrates a mid-voltage single extended N-LDMOSFET with standard gate oxide;

Figure 26b illustrates a mid-voltage single extended N-LDMOSFET with high-voltage gate oxide;

Figure 27a illustrates a mid-voltage floating source N-LDMOSFET with standard gate oxide;

Figure 27b illustrates a mid-voltage floating source N-LDMOSFET with high voltage gate oxide;

Figure 28a illustrates a high-voltage single extended N-MOSFET with standard gate oxide;

Figure 28b illustrates a high-voltage single extended N-MOSFET with high-voltage gate oxide;

Figure 29a illustrates a high-voltage single extended P-MOSFET with standard gate oxide;

Figure 29b illustrates a high-voltage single extended P-MOSFET with high-voltage gate oxide;

Figure 30a illustrates a high-voltage double extended N-MOSFET with standard gate oxide;

Figure 30b illustrates a high-voltage double extended N-MOSFET with high-voltage gate oxide;

Figure 31a illustrates a high-voltage double extended P-MOSFET with standard gate oxide;

Figure 31b illustrates a high-voltage double extended P-MOSFET with high-voltage gate oxide;

Figure 32a illustrates a high-voltage double extended N-LDMOSFET with standard gate oxide;

Figure 32b illustrates a high-voltage double extended N-LDMOSFET with high-voltage gate oxide;

Figure 33a illustrates a very-high-voltage single extended N-LDMOSFET with standard gate oxide;

Figure 33b illustrates a very-high-voltage single extended N-LDMOSFET with high-voltage gate oxide;

Figure 34a illustrates a very-high-voltage single extended P-MOSFET with standard gate oxide;

Figure 34b illustrates a very-high-voltage single extended P-MOSFET with high-voltage gate oxide;

Figure 35a illustrates a very-high-voltage double extended P-MOSFET with standard gate oxide;

Figure 35b illustrates a very-high-voltage double extended P-MOSFET with high-voltage gate oxide;

Figure 36 illustrates a lateral NPN bipolar transistor;

Figure 37 illustrates a high-voltage vertical NPN bipolar transistor;

Figure 38 illustrates a high-voltage vertical PNP bipolar transistor;

Figure 39 illustrates a very-high-gain vertical NPN bipolar transistor;

Figure 40 illustrates a high-voltage N-JFET;

Figure 41a illustrates a very-high-voltage LIGBT with standard gate oxide;

Figure 41b illustrates a very-high-voltage LIGBT with high-voltage gate oxide;

Figure 42 lists the operating voltage range of the 45 active components; and

Figure 43 shows the various junctions characteristics of the various junctions.

## Detailed Description of the Preferred Embodiments

**[0013]** The invention is based on the use of a sixteen mask sequence as shown in the following table.

Table

| Name of Photolithographic Mask | Process Steps |
|---|---|
| Mask 1: N-Well | Starting Material : P- Bulk Silicon |
| | Oxidation (Initial oxide) |
| | Photo |
| | N-Type Implant (N-Well) |
| | Diffusion |
| Mask 2: Active Area | Oxide Etch |
| | Oxidation (Subnitox) |
| | Silicon Nitride Deposition (CVD) |
| | Photo |
| | Nitride Etch |
| Mask 3: P-Field | Photo |
| | P-Type Implant (P-Field) |
| | Blanket N-Type Implant (N-Field) |
| | Oxidation (Field Oxide) |
| | Nitride Etch |
| | Oxide Etch |
| | Oxidation (Pre-Gate Oxide) |
| Mask 4: High-voltage Gate Oxide | Oxide Etch |
| | Oxidation (High-voltage Gate Oxide) |
| | Photo |
| Mask 5: Thin Gate oxide & VTP Adjust | Oxide Etch |
| | Oxidation (Thin Gate Oxide) |
| | Photo |
| | P-Type Implant (VTP Adjust) |
| Mask 6: Polysilicon Gate Patterning | Polysilicon Gate Deposition (CVD) |
| | Polysilicon Doping |
| | Photo |
| | Polysilicon Etch |
| Mask 7: P-Base | Photo |
| | P-Type Implant (P-Base) |
| Mask 8: N-Extended | Photo |
| | N-Type Implant (N-Extended) |
| Mask 9: P-Top | Photo |
| | P-Type Implant (P-Top) |
| Mask 10: N+ Implant | Oxidation and Diffusion |
| | Polysilicon Oxidation |
| | Photo |
| | N-Type Implant (N+) |
| Mask 11: P+ Implant | Photo |
| | P-Type Implant (P+) |
| Mask 12: Contacts | SG/PSG/SOG (Oxide) Deposition |
| | Diffusion |
| | Photo |
| | Contact Etch |
| Mask 13: Metal 1 | Ti/TiN Deposition with Oxidation |
| | Aluminium Alloy Deposition |
| | Photo |
| | Metal Etch |
| | Dielectric and SOG (Oxide) Deposition |
| Mask 14: Vias | Photo |
| | Vias Etch |
| Mask 15: Metal 2 | Ti/TiN Deposition with Oxidation |
| | Aluminium Alloy Deposition |
| | Photo |
| | Metal Etch |
| | Oxide / Nitride Deposition |
| Mask 16: Passivation | Photo |
| | Oxide Etch |

**[0014]** Each mask step is associated with the sub-processes identified in the table. For example, in step 1, starting from bulk P-type silicon, an initial oxidation takes place followed by photolithography to define the mask. An N-type implant takes place to form the N-well, followed by a diffusion step. The sub-processes associated with each remaining step are set forth in the table.

**[0015]** The core of the process that can be used to make numerous diverse components is a basic twelve-mask sequence CMOS process with standard gate oxide consisting of steps 1, 2, 3, 5, 6, 10, 11, 12 13, 14, 15, and 16 as illustrated in Figure 1. This basic twelve- masks CMOS process uses a simple and low cost single P-Type dopant substrate [P-Type bulk substrate or (P-Epitaxial over P+ Bulk substrate)] with standard gate oxide and allows the following six active components to be integrated, namely a standard N-MOSFET with standard gate oxide, as shown in Figure 19a; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a lateral NPN bipolar transistor as shown in Figure 36; a high-voltage vertical PNP bipolar transistor as shown in Figure 38;

**[0016]** Figure 2 shows the various active components that can be achieved with the various combinations of masks of the following standard gate oxide processes:

**[0017]** Figure 3 describes a process which can be used to fabricate in addition to the basic CMOS process of Figure 1 a N-Extended mask (Mask 8: N-Extended) so as to produce a N-Extended thirteen-mask CMOS process with standard gate oxide. As shown in Figure 2, this N-Extended thirteen-mask CMOS process with standard gate oxide allows the integration of another mid-voltage single extended N-MOSFET and of another mid-voltage double-extended N-MOSFET over the six active components of the basic twelve-mask CMOS process with

standard gate oxide so as to provide the integration of the following eight active components, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a mid-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 22a; a mid-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 24a; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30ae; a lateral NPN bipolar transistor as shown in Figure 36; and a high-voltage vertical PNP bipolar transistor as shown in Figure 38;

**[0018]** Figure 4 describes a known process which integrates over the basic CMOS process of Figure 1 a P-Top mask (Mask 9: P-Top) so as to produce a P-Top thirteen-masks Bipolar/CMOS process with standard gate oxide. As shown in Figure 2, this P-Top thirteen-mask Bipolar/CMOS process with standard gate oxide allows the integration of another very-high-gain vertical NPN bipolar transistor and of another high-voltage N-JFET over the six active components of the basic twelve-mask CMOS process with standard gate oxide so as to provide the integration of the eight active components, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a lateral NPN bipolar transistor as shown in Figure 36; a high-voltage vertical PNP bipolar transistor as shown in Figure 38; a very-high-gain vertical NPN bipolar transistor as shown in Figure 39; and a high-voltage N-JFET as shown in Figure 40.

**[0019]** Figure 5 describes a process which integrates over the basic CMOS process of Figure 1 the combination of a N-Extended mask (Mask 8: N-Extended) and of a P-Top mask (Mask 9: P-Top) so as to produce a N-Extended and P-Top fourteen-mask Bipolar/CMOS process with standard gate oxide. As shown in Figure 2,

this N-Extended and P-Top fourteen-mask Bipolar/CMOS process with standard gate oxide allows the integration of the other two active components of the N-Extended thirteen-mask CMOS process with standard gate oxide as well as of the other two active components of the P-Top thirteen-mask Bipolar/CMOS process with standard gate oxide over the six active components of the basic twelve-mask CMOS process with standard gate oxide so as to provide the integration of the ten active components, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a mid-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 22a; a mid-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 24a; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a lateral NPN bipolar transistor as shown in Figure 36; a high-voltage vertical PNP bipolar transistor as shown in Figure 38; a very-high-gain vertical NPN bipolar transistor as shown in Figure 39; and a high-voltage N-JFET as shown in Figure 40.

**[0020]** Figure 6 describes a process which integrates over the basic CMOS process of Figure 1 a P-Base mask (Mask 7: P-Base) so as to produce a P-Base thirteen-masks Bipolar/CMOS/DMOS process with standard gate oxide. As shown in Figure 2, this P-Base thirteen-mask Bipolar/CMOS/DMOS process with standard gate oxide allows the integration of another standard Junction isolated N-MOSFET, of another mid-voltage single extended P-MOSFET, of another mid-voltage double extended P-MOSFET, of another mid-voltage single extended N-LDMOSFET, of another mid-voltage floating source N-LDMOSFET and of another high-voltage vertical NPN bipolar transistor over the six active components of the basic twelve-mask CMOS process with standard gate oxide so as to provide the integration of the twelve active components, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a standard Junction

isolated N-MOSFET with standard gate oxide as shown in Figure 21a; a mid-voltage single extended P-MOSFET with standard gate oxide a Figure 23a; a mid-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 25a; a mid-voltage single extended N-LDMOSFET with standard gate oxide as shown in Figure 26a; a mid-voltage floating source N-LDMOSFET with standard gate oxide as shown in Figure 27a; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a lateral NPN bipolar transistor as shown in Figure 36; a high-voltage vertical NPN bipolar transistor as shown in Figure 37; and a high-voltage vertical PNP bipolar transistor as shown in Figure 38.

**[0021]** Figure 7 describes a process which integrates over the basic CMOS process of Figure 1 the combination of a P-Base mask (Mask 7: P-Base) and of a N-Extended mask (Mask 8: N-Extended) so as to produce a P-Base and N-Extended fourteen-masks Bipolar/CMOS/DMOS process with standard gate oxide. As shown in Figure 2, this P-Base and N-Extended fourteen-mask Bipolar/CMOS/DMOS process with standard gate oxide allows the integration of the other six active components of the P-Base thirteen-mask Bipolar/CMOS/DMOS process with standard gate oxide and of the other two active components of the N-Extended thirteen-mask CMOS process with standard gate oxide over the six active components of the basic twelve-mask CMOS process with standard gate oxide so as to provide the integration of the fourteen active components, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a standard Junction isolated N-MOSFET with standard gate oxide as shown in Figure 21a; a mid-voltage single extended N-MOSFET with standard gate oxide as show in Figure 22a; a mid-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 23aa mid-voltage double extended N-MOSFET with standard gate oxide as shown in ; Figure 24a; a mid-voltage double extended P-MOSFET with standard gate oxide as shown in Figure

25a; a mid-voltage single extended N-LDMOSFET with standard gate oxide as shown in Figure 26a; a mid-voltage floating source N-LDMOSFET with standard gate oxide as shown in Figure 27a; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a lateral NPN bipolar transistor as shown in ; Figure 37 a high-voltage vertical NPN bipolar transistor as shown in Figure 36; and a high-voltage vertical PNP bipolar transistor as shown in Figure 38.

**[0022]** Figure 8 describes a process which integrates over the basic CMOS process of Figure 1 the combination of a P-Base mask (Mask 7: P-Base) and of a P-Top mask (Mask 9: P-Top) so as to produce a P-Base and P-Top fourteen-mask Bipolar/CMOS/DMOS process with standard gate oxide.

**[0023]** As shown in Figure 2, this P-Base and P-Top fourteen-mask Bipolar/CMOS/DMOS process with standard gate oxide allows the integration of the other six active components of the P-Base thirteen-mask Bipolar/CMOS/DMOS process with standard gate oxide, of the other two active components of the P-Top thirteen-mask Bipolar/CMOS process with standard gate oxide, of another high-voltage single extended P-MOSFET, of another high-voltage double extended P-MOSFET, of another high-voltage double extended N-LDMOSFET, of another very-high-voltage single extended N-LDMOSFET, of another very-high-voltage single extended P-MOSFET, of another very-high-voltage double extended P-MOSFET, and of another very-high-voltage Lateral Insulated Gate Bipolar transistor LIGBT over the six active components of the basic twelve-mask CMOS process with standard gate oxide so as to provide the integration of twenty-one active components, namely a standard N-MOSFET with standard gate oxide is shown in Figure 19a; a standard P-MOSFET with standard gate oxide is shown in Figure 20a; a standard Junction isolated N-MOSFET with standard gate oxide is shown in Figure 21a; a mid-voltage single extended P-MOSFET with standard gate oxide is shown in Figure 23a; a mid-voltage double extended P-MOSFET with standard gate oxide is shown in Figure

25a; a mid-voltage single extended N-LDMOSFET with standard gate oxide is shown in Figure 26a; a mid-voltage floating source N-LDMOSFET with standard gate oxide is shown in Figure 27a; a high-voltage single extended N-MOSFET with standard gate oxide is shown in Figure 28a; a high-voltage single extended P-MOSFET with standard gate oxide Figure 30a a high-voltage double extended N-MOSFET with standard gate oxide is shown in Figure 29a; a high-voltage double extended P-MOSFET with standard gate oxide is shown in Figure 31a; a high-voltage double extended N-LDMOSFET with standard gate oxide is shown in Figure 32a; a very-high-voltage single extended N-LDMOSFET with standard gate oxide is shown in Figure 33a; a very-high-voltage single extended P-MOSFET with standard gate oxide is shown in Figure 34a; a very-high-voltage double extended P-MOSFET with standard gate oxide Figure 36 a lateral NPN bipolar transistor is shown in Figure 35a; a high-voltage vertical NPN bipolar transistor is shown in Figure 37; a high-voltage vertical PNP bipolar transistor is shown in Figure 38; a very-high-gain vertical NPN bipolar transistor is shown in Figure 39; a high-voltage N-JFET is shown in Figure 40; And a very-high-voltage Lateral Insulated Gate Bipolar transistor LIGBT with standard gate oxide as shown in Figure 41a.

**[0024]** Figure 9 describes a very important aspect of the process which integrates over the basic CMOS process of Figure 1 the combination of a P-Base mask (Mask 7: P-Base), of a N-Extended mask (Mask 8: N-Extended) and of a P-Top mask (Mask 9: P-Top) as to produce a P-Base, N-Extended and P-Top fifteen- mask Bipolar/CMOS/DMOS process with standard gate oxide.

**[0025]** As shown on Figure 2, this P-Base, N-Extended and P-Top fifteen-mask Bipolar/CMOS/DMOS process with standard gate oxide allows the integration of the other fifteen active components of the P-Base and P-Top fourteen-mask Bipolar/CMOS/DMOS process with standard gate oxide and of the other two active components of the N-Extended thirteen-mask CMOS process with standard gate oxide over the six active components of the basic twelve-mask CMOS process with standard gate oxide so as to provide the integration of the f

twenty-three active components, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a ; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a standard Junction isolated N-MOSFET with standard gate oxide as shown in Figure 21a; a mid-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 22a; a mid-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 23a; a mid-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 24a; a mid-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 25a; a mid-voltage single extended N-LDMOSFET with standard gate oxide as shown in Figure 26a; a mid-voltage floating source N-LDMOSFET with standard gate oxide as shown in Figure 27a; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 29a; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a high-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 31a; a high-voltage double extended N-LDMOSFET with standard gate oxide as shown in Figure 32a; a very-high-voltage single extended N-LDMOSFET with standard gate oxide as shown in Figure 33a; a very-high-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 34a; a very-high-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 35a; a lateral NPN bipolar transistor as shown in Figure 36; a high-voltage vertical NPN bipolar transistor as shown in Figure 37; a high-voltage vertical PNP bipolar transistor as shown in Figure 38; a very-high-gain vertical NPN bipolar transistor as shown in Figure 39; a high-voltage N-JFET as shown in Figure 40; and a very-high-voltage Lateral Insulated Gate Bipolar transistor LIGBT with standard gate oxide as shown in Figure 41a.

**[0026]** Figure 10 lists the various active components obtained by a process in accordance with the invention with the various combinations of masks of the following dual (standard and high-voltage) gate oxide processes:

[0027] Figure 11 describes a known process which integrates over the basic CMOS process of Figure 1 a High-voltage mask (Mask 4: High-voltage Gate Oxide) so as to produce a Dual gate oxide basic thirteen-mask CMOS process. As shown in Figure 2 and Figure 10, this Dual gate oxide basic thirteen-mask CMOS process allows the integration of another standard N-MOSFET with high-voltage gate oxide, of another standard P-MOSFET with high-voltage gate oxide, of another high-voltage single extended N-MOSFET with high-voltage gate oxide and of another high-voltage double extended N-MOSFET with high-voltage gate oxide over the basic twelve-mask CMOS process with standard gate oxide so as to provide the integration of the ten active components, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a ; a standard N-MOSFET with high-voltage gate oxide as shown in Figure 19b; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a standard P-MOSFET with high-voltage gate oxide as shown in Figure 20b; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage single extended N-MOSFET with high-voltage gate oxide as shown in Figure 28b; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a high-voltage double extended N-MOSFET with high-voltage gate oxide as shown in Figure 30b; a lateral NPN bipolar transistor as shown in Figure 36; and a high-voltage vertical PNP bipolar transistor as shown in Figure 38.

[0028] Figure 12 describes a process which integrates over the basic CMOS process of Figure 1 a High-voltage mask (Mask 4: High-voltage Gate Oxide) and a P-Top mask (Mask 9: P-Top) so as to produce a Dual gate oxide P-Top fourteen-mask Bipolar/CMOS process. As shown in Figure 2 and Figure 10, this Dual gate oxide P-Top fourteen-mask Bipolar/CMOS process allows the integration of the two other components of the P-Top thirteen-mask CMOS process with standard gate oxide over the ten active components of the Dual gate oxide basic thirteen-mask CMOS process so as to provide the integration of the twelve active components, namely a standard N-MOSFET with standard gate oxide as shown

in Figure 19a; a standard N-MOSFET with high-voltage gate oxide as shown in Figure 19b; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a standard P-MOSFET with high-voltage gate oxide as shown in Figure 20b; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage single extended N-MOSFET with high-voltage gate oxide as shown in Figure 28b; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a high-voltage double extended N-MOSFET with high-voltage gate oxide as shown in Figure 30b; a lateral NPN bipolar transistor as shown in Figure 36; a high-voltage vertical PNP bipolar transistor as shown in Figure 38; a very-high-gain vertical NPN bipolar transistor as shown in Figure 39; and a high-voltage N-JFET as shown in Figure 40.

**[0029]** Figure 13 describes a known process which integrates over the basic CMOS process of Figure 1 a High-voltage mask (Mask 4: High-voltage Gate Oxide) and a N-Extended mask (Mask 8: N-Extended) so as to produce a Dual gate oxide N-Extended fourteen-mask CMOS process. As shown in Figure 2 and Figure 10, this Dual gate oxide N-Extended fourteen-mask CMOS process allows the integration of the two other components of the N-Extended thirteen-mask CMOS process with standard gate oxide, of another mid-voltage single extended N-MOSFET with high-voltage gate oxide and of another mid-voltage double extended N-MOSFET with high-voltage gate over the ten active components of the Dual gate oxide basic thirteen-mask CMOS process so as to provide the integration of the fourteen active components, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a; a standard N-MOSFET with high-voltage gate oxide as shown in Figure 19b; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a standard P-MOSFET with high-voltage gate oxide as shown in Figure 20b; a mid-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 22a; a mid-voltage single extended N-MOSFET with high-voltage gate oxide as shown in Figure 22b; a mid-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 24a; a mid-voltage double extended N-MOSFET with high-voltage gate

oxide as shown in Figure 24b; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage single extended N-MOSFET with high-voltage gate oxide as shown in Figure 28ba high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a high-voltage double extended N-MOSFET with high-voltage gate oxide as shown in Figure 30b; a lateral NPN bipolar transistor as shown in Figure 36; and a high-voltage vertical PNP bipolar transistor as shown in Figure 38.

**[0030]** Figure 14 describes a process which integrates over the basic CMOS process of Figure 1 a High-voltage mask (Mask 4: High-voltage Gate Oxide), a N-Extended mask (Mask 8: N-Extended) and a P-Top mask (Mask 9: P-Top) so as to produce a Dual gate oxide N-Extended and P-Top fifteen-mask Bipolar/CMOS process. As shown in Figure 2 and Figure 10, this Dual gate oxide N-Extended and P-Top fifteen-mask Bipolar/CMOS process allows the integration of the other four active components of the Dual gate oxide N-Extended fourteen-masks CMOS process and of the other two active components of the Dual gate oxide P-Top fourteen-masks Bipolar/CMOS process over the ten active components of the Dual gate oxide basic thirteen-mask CMOS process so as to provide the integration of the sixteen active components, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a; a standard N-MOSFET with high-voltage gate oxide as shown in Figure 19b; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a standard P-MOSFET with high-voltage gate oxide as shown in Figure 20b; a mid-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 22a; a mid-voltage single extended N-MOSFET with high-voltage gate oxide as shown in Figure 22b; a mid-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 24a; a mid-voltage double extended N-MOSFET with high-voltage gate oxide as shown in Figure 24b; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage single extended N-MOSFET with high-voltage gate oxide as shown in Figure 28b; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a

high-voltage double extended N-MOSFET with high-voltage gate oxide as shown in Figure 30b;a lateral NPN bipolar transistor as shown in Figure 36; a high-voltage vertical PNP bipolar transistor as shown in Figure 38; a very-high-gain vertical NPN bipolar transistor as shown in Figure 39; and a high-voltage N-JFET as shown in Figure 40.

**[0031]** Figure 15 describes a process which integrates over the basic CMOS process of Figure 1 a High-voltage mask (Mask 4: High-voltage Gate Oxide) and a P-Base mask (Mask 7: P-Base) so as to produce a Dual gate oxide P-Base fourteen-mask Bipolar/CMOS/DMOS process. As shown in Figure 2 and Figure 10, this Dual gate oxide P-Base fourteen-mask Bipolar/CMOS/DMOS process allows the integration of the other six other components of the P-Base thirteen-mask Bipolar/CMOS/DMOS process with standard gate oxide, of another standard Junction isolated N-MOSFET with high-voltage gate oxide, of another mid-voltage single extended P-MOSFET with high-voltage gate oxide, of another mid-voltage double extended P-MOSFET with high-voltage gate oxide, of another mid-voltage single extended N-LDMOSFET with high-voltage gate oxide and of another mid-voltage floating source N-LDMOSFET with high-voltage gate oxide over the ten active components of the Dual gate oxide basic thirteen-mask CMOS process so as to provide the integration of the following twenty-one (21) active components, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a; a standard N-MOSFET with high-voltage gate oxide as shown in Figure 19b; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a standard P-MOSFET with high-voltage gate oxide as shown in Figure 20b; a standard Junction isolated N-MOSFET with standard gate oxide as shown in Figure 21a; a standard Junction isolated N-MOSFET with high-voltage gate oxide as shown in Figure 21b; a mid-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 23a; a mid-voltage single extended P-MOSFET with high-voltage gate oxide as shown in Figure 23b; a mid-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 25a; a mid-voltage double extended P-MOSFET with high-voltage gate oxide as shown

in Figure 25b; a mid-voltage single extended N-LDMOSFET with standard gate oxide as shown in Figure 26a; a mid-voltage single extended N-LDMOSFET with high-voltage gate oxide as shown in Figure 26b; a mid-voltage floating source N-LDMOSFET with standard gate oxide as shown in Figure 27a; a mid-voltage floating source N-LDMOSFET with high-voltage gate oxide as shown in Figure 27b; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage single extended N-MOSFET with high-voltage gate oxide as shown in Figure 28b; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a high-voltage double extended N-MOSFET with high-voltage gate oxide as shown in Figure 30b; a lateral NPN bipolar transistor as shown in Figure 36; a high-voltage vertical NPN bipolar transistor as shown in Figure 37; and a high-voltage vertical PNP bipolar transistor as shown in Figure 38.

**[0032]** Figure 16 describes an important process which integrates over the basic CMOS process of Figure 1 a High-voltage mask (Mask 4: High-voltage Gate Oxide), a P-Base mask (Mask 7: P-Base) and a N-Extended mask (Mask 8: N-Extended) so as to produce a Dual gate oxide P-Base and N-Extended fifteen-mask Bipolar/CMOS/DMOS process. As shown in Figure 2 and Figure 10, this Dual gate oxide P-Base and N-Extended fifteen-mask Bipolar/CMOS/DMOS process allows the integration of the other eleven active components of the Dual gate oxide P-Base fourteen-mask Bipolar/CMOS/DMOS process and of the other four active components of the Dual gate oxide N-Extended fourteen-mask CMOS process over the ten active components of the Dual gate oxide basic thirteen-mask CMOS process as to provide the integration of twenty-five active components, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a ; a standard N-MOSFET with high-voltage gate oxide as shown in Figure 19b; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a standard P-MOSFET with high-voltage gate oxide as shown in Figure 20b; a standard Junction isolated N-MOSFET with standard gate oxide as shown in Figure 21a; a standard Junction isolated N-MOSFET with high-voltage gate oxide

as shown in Figure 21b; a mid-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 22a; a mid-voltage single extended N-MOSFET with high-voltage gate oxide as shown in Figure 22b; a mid-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 23a; a mid-voltage single extended P-MOSFET with high-voltage gate oxide as shown in Figure 23b; a mid-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 24a; a mid-voltage double extended N-MOSFET with high-voltage gate oxide as shown in Figure 24b; a mid-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 25a; a mid-voltage double extended P-MOSFET with high-voltage gate oxide as shown in Figure 25b; a mid-voltage single extended N-LDMOSFET with standard gate oxide; as shown in Figure 26a; a mid-voltage single extended N-LDMOSFET with high-voltage gate oxide as shown in Figure 26b; a mid-voltage floating source N-LDMOSFET with standard gate oxide as shown in Figure 27a; a mid-voltage floating source N-LDMOSFET with high-voltage gate oxide as shown in Figure 27b; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage single extended N-MOSFET with high-voltage gate oxide as shown in Figure 28b; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a high-voltage double extended N-MOSFET with high-voltage gate oxide as shown in Figure 30b; a lateral NPN bipolar transistor as shown in Figure 36; a high-voltage vertical NPN bipolar transistor as shown in Figure 37; and a high-voltage vertical PNP bipolar transistor as shown in Figure 38.

**[0033]** Figure 17 describes an important process which integrates over the basic CMOS process of Figure 1 a High-voltage mask (Mask 4: High-voltage Gate Oxide), a P-Base mask (Mask 7: P-Base) and a P-Top mask (Mask 9: P-Top) so as to produce a Dual gate oxide P-Base and P-Top fifteen-mask Bipolar/CMOS/DMOS process. As shown in Figure 2 and Figure 10, this Dual gate oxide P-Base and P-Top fifteen-mask Bipolar/CMOS/DMOS process allows the integration of the other eleven active components of the Dual gate oxide P-

Base fourteen-mask Bipolar/CMOS/DMOS process, of the other two active components of the Dual gate oxide P-Top fourteen-mask Bipolar/CMOS process, of the other seven active components of the P-Base and P-Top fourteen-mask Bipolar/CMOS/DMOS process with standard gate oxide, of another high-voltage single extended P-MOSFET with high-voltage gate oxide, of another high-voltage double extended P-MOSFET with high-voltage gate oxide, of another high-voltage double extended N-LDMOSFET with high-voltage gate oxide, of another very-high-voltage single extended N-LDMOSFET with high-voltage gate oxide, of another very-high-voltage single extended P-MOSFET with high-voltage gate oxide, of another very-high-voltage double extended P-MOSFET with high-voltage gate oxide and of another very-high-voltage Lateral Insulated Gate Bipolar transistor LIGBT with high-voltage gate oxide over the ten active components of the Dual gate oxide basic thirteen-mask CMOS process so as to provide the integration of the thirty-seven active components, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a; a standard N-MOSFET with high-voltage gate oxide as shown in Figure 19b; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a standard P-MOSFET with high-voltage gate oxide as shown in Figure 20b; a standard Junction isolated N-MOSFET with standard gate oxide as shown in Figure 21aa standard Junction isolated N-MOSFET with high-voltage gate oxide as shown in ; Figure 21b; a mid-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 23a; a mid-voltage single extended P-MOSFET with high-voltage gate oxide as shown in Figure 23b; a mid-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 25a; a mid-voltage double extended P-MOSFET with high-voltage gate oxide as shown in Figure 25b; a mid-voltage single extended N-LDMOSFET with standard gate oxide as shown in Figure 26a; a mid-voltage single extended N-LDMOSFET with high-voltage gate oxide as shown in Figure 26b; a mid-voltage floating source N-LDMOSFET with standard gate oxide as shown in Figure 27a; a mid-voltage floating source N-LDMOSFET with high-voltage gate oxide as shown in Figure 27b; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a

high-voltage single extended N-MOSFET with high-voltage gate oxide as shown in Figure 28b; a high-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 29a; a high-voltage single extended P-MOSFET with high-voltage gate oxide as shown in Figure 29b; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a high-voltage double extended N-MOSFET with high-voltage gate oxide as shown in Figure 30b; a high-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 31a; a high-voltage double extended P-MOSFET with high-voltage gate oxide as shown in Figure 31b; a high-voltage double extended N-LDMOSFET with standard gate oxide as shown in Figure 32a; a high-voltage double extended N-LDMOSFET with high-voltage gate oxide as shown in Figure 32b; a very-high-voltage single extended N-LDMOSFET with standard gate oxide as shown in Figure 33a; a very-high-voltage single extended N-LDMOSFET with high-voltage gate oxide as shown in Figure 33b; a very-high-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 34a; a very-high-voltage single extended P-MOSFET with high-voltage gate oxide as shown in Figure 34b; a very-high-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 35a; a very-high-voltage double extended P-MOSFET with high-voltage gate oxide as shown in Figure 35b; a lateral NPN bipolar transistor as shown in Figure 36; a high-voltage vertical NPN bipolar transistor as shown in Figure 37; a high-voltage vertical PNP bipolar transistor as shown in Figure 38; a very-high-gain vertical NPN bipolar transistor as shown in Figure 39; a high-voltage N-JFET as shown in Figure 40; a very-high-voltage Lateral Insulated Gate Bipolar transistor LIGBT with standard gate oxide as shown in Figure 41a; and a very-high-voltage Lateral Insulated Gate Bipolar transistor LIGBT with high-voltage gate oxide as shown in Figure 41b.

**[0034]** Figure 18 describes an important process which integrates over the basic CMOS process of Figure 1 a High-voltage mask (Mask 4: High-voltage Gate Oxide), a P-Base mask (Mask 7: P-Base), a N-Extended mask (Mask 8: N-Extended) and a P-Top mask (Mask 9: P-Top) as to produce a Dual gate oxide P-

Base, N-Extended and P-Top sixteen-mask Bipolar/CMOS/DMOS process. As shown in Figure 2 and Figure 10, this Dual gate oxide P-Base, N-Extended and P-Top sixteen-mask Bipolar/CMOS/DMOS process allows the integration of the other twenty-seven active components of the Dual gate oxide P-Base and P-Top fifteen-mask Bipolar/CMOS/DMOS process, of the other two active components of the N-Extended thirteen-mask CMOS process with standard gate oxide, of another mid-voltage single extended N-MOSFET with high-voltage gate oxide and of another mid-voltage double extended N-MOSFET with high-voltage gate oxide over the ten active components of the Dual gate oxide basic thirteen-mask CMOS process so as to provide the integration of the forty-one active components, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a; a standard N-MOSFET with high-voltage gate oxide as shown in Figure 19b; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a standard P-MOSFET with high-voltage gate oxide as shown in Figure 20b; a standard Junction isolated N-MOSFET with standard gate oxide as shown in Figure 21a; a standard Junction isolated N-MOSFET with high-voltage gate oxide as shown in Figure 21b; a mid-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 22a; a mid-voltage single extended N-MOSFET with high-voltage gate oxide as shown in Figure 22b; a mid-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 23a; a mid-voltage single extended P-MOSFET with high-voltage gate oxide as shown in Figure 23b; a mid-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 24a; a mid-voltage double extended N-MOSFET with high-voltage gate oxide as shown in Figure 24b; a mid-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 25a; a mid-voltage double extended P-MOSFET with high-voltage gate oxide as shown in Figure 25b; a mid-voltage single extended N-LDMOSFET with standard gate oxide as shown in Figure 26a; a mid-voltage single extended N-LDMOSFET with high-voltage gate oxide as shown in Figure 26b;a mid-voltage floating source N-LDMOSFET with standard gate oxide as shown in Figure 27a;a mid-voltage floating source N-LDMOSFET with high-voltage gate oxide as shown in Figure 27b; a high-voltage

single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage single extended N-MOSFET with high-voltage gate oxide as shown in Figure 28b; a high-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 29a; a high-voltage single extended P-MOSFET with high-voltage gate oxide as shown in Figure 29b; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a high-voltage double extended N-MOSFET with high-voltage gate oxide as shown in Figure 30b; a high-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 31a; a high-voltage double extended P-MOSFET with high-voltage gate oxide as shown in Figure 31b; a high-voltage double extended N-LDMOSFET with standard gate oxide as shown in Figure 32a; a high-voltage double extended N-LDMOSFET with high-voltage gate oxide as shown in Figure 32b; a very-high-voltage single extended N-LDMOSFET with standard gate oxide as shown in Figure 33a; a very-high-voltage single extended N-LDMOSFET with high-voltage gate oxide as shown in Figure 33b; a very-high-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 34a; a very-high-voltage single extended P-MOSFET with high-voltage gate oxide as shown in Figure 34b; a very-high-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 35a; a very-high-voltage double extended P-MOSFET with high-voltage gate oxide as shown in Figure 35b; a lateral NPN bipolar transistor as shown in Figure 36; a high-voltage vertical NPN bipolar transistor as shown in Figure 37; a high-voltage vertical PNP bipolar transistor as shown in Figure 38; a very-high-gain vertical NPN bipolar transistor as shown in Figure 39; a high-voltage N-JFET as shown in Figure 40; a very-high-voltage Lateral Insulated Gate Bipolar transistor LIGBT with standard gate oxide as shown in Figure 41a; and a very-high-voltage Lateral Insulated Gate Bipolar transistor LIGBT with high-voltage gate oxide as shown in Figure 41b.

**[0035]** It is clear from Figure 9 that the P-Base, N-Extended and P-Top Bipolar/CMOS/DMOS process with standard gate oxide is an extremely flexible process since the combinations of P-Base, N-Extended and P-Top masks allow

the designer to combine the twenty-three different active components into an integrated circuit without having to deal with multiple circuits or with complex processes, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a standard Junction isolated N-MOSFET with standard gate oxide as shown in Figure 21a; a mid-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 22a; a mid-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 23a; a mid-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 24a; a mid-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 25a; a mid-voltage single extended N-LDMOSFET with standard gate oxide as shown in Figure 26a; a mid-voltage floating source N-LDMOSFET with standard gate oxide as shown in Figure 27aa high-voltage single extended N-MOSFET with standard gate oxide as shown in ; Figure 28a; a high-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 29a; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a high-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 31a; a high-voltage double extended N-LDMOSFET with standard gate oxide as shown in Figure 32a; a very-high-voltage single extended N-LDMOSFET with standard gate oxide as shown in Figure 33a; a very-high-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 34a; a very-high-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 35a; a lateral NPN bipolar transistor as shown in Figure 36; a high-voltage vertical NPN bipolar transistor as shown in Figure 37; a high-voltage vertical PNP bipolar transistor as shown in Figure 38; a very-high-gain vertical NPN bipolar transistor as shown in Figure 39; a high-voltage N-JFET as shown in Figure 40; and a very-high-voltage Lateral Insulated Gate Bipolar transistor LIGBT with standard gate oxide as shown in Figure 41a.

**[0036]** It is clear from Figure 42 and Figure 43 that these twenty-three different active components are associated with very different operating voltage

characteristics. They are also associated with a wide variety of other electrical performances such as breakdown voltage, cut-off frequency, specific channel resistance, size figure-of-merit, which allows the designer to cherry-pick the ideal combination of active components for a given application and to cherry-pick another different combination of active components for another application.

**[0037]** Again, this invention provides an extremely versatile set of active components for the designer which allow the integration of components which would otherwise be achieved using independent substrates and/or much more complex processes.

**[0038]** It is clear from Figure 18 that the Dual gate oxide P-Base, N-Extended and P-Top Bipolar/CMOS/DMOS process is an extremely flexible process since the combinations of P-Base, N-Extended and P-Top masks allow the designer to combine the forty-one different active components into an integrated circuit without having to deal with multiple circuits or with much more complex processes, namely a standard N-MOSFET with standard gate oxide as shown in Figure 19a; a standard N-MOSFET with high-voltage gate oxide as shown in Figure 19b; a standard P-MOSFET with standard gate oxide as shown in Figure 20a; a standard P-MOSFET with high-voltage gate oxide as shown in Figure 20b; a standard Junction isolated N-MOSFET with standard gate oxide as shown in Figure 21a; a standard Junction isolated N-MOSFET with high-voltage gate oxide as shown in Figure 21b; a mid-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 22a; a mid-voltage single extended N-MOSFET with high-voltage gate oxide as shown in Figure 22b; a mid-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 23a; a mid-voltage single extended P-MOSFET with high-voltage gate oxide as shown in Figure 23b; a mid-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 24a; a mid-voltage double extended N-MOSFET with high-voltage gate oxide as shown in Figure 24b; a mid-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 25a; a mid-voltage double extended P-MOSFET with high-voltage gate oxide as shown in Figure 25b; a mid-

voltage single extended N-LDMOSFET with standard gate oxide as shown in Figure 26a; a mid-voltage single extended N-LDMOSFET with high-voltage gate oxide as shown in Figure 26b; a mid-voltage floating source N-LDMOSFET with standard gate oxide as shown in Figure 27a; a mid-voltage floating source N-LDMOSFET with high-voltage gate oxide; as shown in Figure 27b; a high-voltage single extended N-MOSFET with standard gate oxide as shown in Figure 28a; a high-voltage single extended N-MOSFET with high-voltage gate oxide as shown in Figure 28b; a high-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 29a; a high-voltage single extended P-MOSFET with high-voltage gate oxide as shown in Figure 29b; a high-voltage double extended N-MOSFET with standard gate oxide as shown in Figure 30a; a high-voltage double extended N-MOSFET with high-voltage gate oxide as shown in Figure 30b; a high-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 31a; a high-voltage double extended P-MOSFET with high-voltage gate oxide as shown in Figure 31b; a high-voltage double extended N-LDMOSFET with standard gate oxide as shown in Figure 32a; a high-voltage double extended N-LDMOSFET with high-voltage gate oxide as shown in Figure 32b; a very-high-voltage single extended N-LDMOSFET with standard gate oxide as shown in Figure 33a; a very-high-voltage single extended N-LDMOSFET with high-voltage gate oxide as shown in Figure 33b; a very-high-voltage single extended P-MOSFET with standard gate oxide as shown in Figure 34a; a very-high-voltage single extended P-MOSFET with high-voltage gate oxide as shown in Figure 34b; a very-high-voltage double extended P-MOSFET with standard gate oxide as shown in Figure 35a; a very-high-voltage double extended P-MOSFET with high-voltage gate oxide as shown in Figure 35b; a lateral NPN bipolar transistor as shown in Figure 36a high-voltage vertical NPN bipolar transistor as shown in ; Figure 37; a high-voltage vertical PNP bipolar transistor as shown in Figure 38; a very-high-gain vertical NPN bipolar transistor as shown in Figure 39; a high-voltage N-JFET as shown in Figure 40; a very-high-voltage Lateral Insulated Gate Bipolar transistor LIGBT with standard gate oxide as

shown in Figure 41a; and a very-high-voltage Lateral Insulated Gate Bipolar transistor LIGBT with high-voltage gate oxide as shown in Figure 41b.

**[0039]** Again, it is clear from Figure 42 and Figure 43 that these forty-one different active components are associated with very different operating voltage characteristics. They are also associated with a wide variety of other electrical performances such as breakdown voltage, cut-off frequency, specific channel resistance, size figure-of-merit, which allows the designer to cherry-pick the ideal combination of active components for a given application and to cherry-pick another different combination of active components for another application using this unique process.

**[0040]** The novel process provides an extremely versatile set of active components for the designer which allow the integration of components which would otherwise be achieved using independent substrates and/or much more complex processes.

**[0041]** The invention can be practiced on a Silicon Over Isolator (SOI) substrate and achieve higher breakdown voltage up to about 1200 volts for the following active components if the silicon layer over the buried oxide is thicker then 1.5 μm: a high-voltage double extended N-LDMOSFET shown in Figure 32a; a high-voltage double extended N-LDMOSFET shown in Figure 32b; a very-high-voltage single extended N-LDMOSFET shown in Figure 33a; a very-high-voltage single extended N-LDMOSFET shown in Figure 33b; a very-high-voltage single extended P-MOSFET shown in Figure 34a; a very-high-voltage single extended P-MOSFET shown in Figure 34b; a very-high-voltage double extended P-MOSFET shown in Figure 35a; a very-high-voltage double extended P-MOSFET shown in Figure 35b; and a high-voltage N-JFET shown in Figure 40.

**[0042]** Similarly, the maximum operating drain voltage of the following active components could be increased to 1200 volts if the resistivity of the various layers is optimized: the high-voltage double extended N-LDMOSFET of Figure 32a; the high-voltage double extended N-LDMOSFET of Figure 32b; the very-high-

voltage single extended N-LDMOSFET of Figure 33a; the very-high-voltage single extended N-LDMOSFET of Figure 33b; the very-high-voltage single extended P-MOSFET of Figure 34a; the very-high-voltage single extended P-MOSFET of Figure 34b; the very-high-voltage double extended P-MOSFET of Figure 35a; and the very-high-voltage double extended P-MOSFET of Figure 35b; the high-voltage N-JFET of Figure 40;

**[0043]** The lower voltage range of 3.3 volts of the following active components could be reduced down to 2.5 volts if the speed reduction associated with the gate operation voltage of 2.5 volts is high enough for the application: the standard N-MOSFETs of Figure 19a; the standard N-MOSFETs of Figure 19b; the standard P-MOSFETs of Figure 20a; the standard P-MOSFETs of Figure 20b; the standard Junction isolated N-MOSFETs of Figure 21a; and the standard Junction isolated N-MOSFETs of Figure 21b.

**[0044]** The invention finds application in analog devices and/or integrated circuit requiring a mix of transistors characteristics and/or operation voltages; mixed-signal devices and/or integrated circuit requiring a mix of transistors characteristics and/or operation voltages; Bipolar devices and/or integrated circuit requiring a mix of transistors characteristics and/or operation voltages; CMOS devices and/or integrated circuit requiring a mix of transistors characteristics and/or operation voltages; DMOS devices and/or integrated circuit requiring a mix of transistors characteristics and/or operation voltages; Bi-CMOS devices and/or integrated circuit requiring a mix of transistors characteristics and/or operation voltages; Micro-Electro-Mechanical Systems (MEMS) requiring a mix of transistors characteristics and/or operation voltages; Micro-Opto-Electro-Mechanical Systems (MOEMS) requiring a mix of transistors characteristics and/or operation voltages; biological or medical devices and/or circuits such as biochips, laboratory-on-a-chip (LOAC) or micro-total analysis systems (μ-TAS) requiring a mix of transistors characteristics and/or operation voltages; charged Coupled Devices (CCD) devices and/or circuits requiring a mix of transistors characteristics and/or operation voltages; and CCD/CMOS

devices and/or circuits requiring a mix of transistors characteristics and/or operation voltages. This is not an exhaustive list. Other applications will be apparent to one skilled in the art.

**[0045]** The embodiments presented are exemplary only and persons skilled in the art would appreciate that variations to the above described embodiments may be made without departing from the spirit of the invention. The scope of the invention is solely defined by the appended claims.